UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,766	03/27/2001	Masakazu Taguchi	0941.65368	2399

7590 05/19/2004

Patrick G. Burns, Esq.
GREER, BURNS & CRAIN, LTD.
Suite 2500
300 South Wacker Dr.
Chicago, IL 60606

EXAMINER	
RODRIGUEZ, GLENDA P	
ART UNIT	**PAPER NUMBER**
2651	7

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/818,766	Applicant(s) TAGUCHI ET AL.	
	Examiner Glenda P. Rodriguez	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. Pat. No. 5, 056, 116) in view of Byrne et al. (U.S. Pat. No. 6, 487, 672) and Sprague (US Patent No. 6, 072, 645).

Regarding Claims 1, 4 and 5, Shimada et al. disclose an apparatus for reading recorded data, said apparatus comprising:

> A first clock generating part generating a first clock signal and a second clock signal generating part generating a second clock signal different from the first clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.);

A sampling part sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal (Pat. No. 5, 056, 116; Col. 4, Lines 52-57);

A first storing part consecutively storing a sample value obtained by said sampling part (Pat. No. 5, 056, 116; See Fig. 22. Shimada et al. disclose that the analog to digital converter (Element 1) supplies the sampled signal to a buffer (Element 15), which is a storing part);

A data detecting part retrieving the sample value from said first storing part by synchronizing a second clock signal different from the first clock signal and detecting data by processing the sample value in accordance with a predetermined algorithm, so that the recorded data is read based on the data detected by said data detecting part (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.).

Shimada et al. also disclose that the data detecting part is synchronized with a second clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.). Shimada et al. fail to disclose that the

detector retrieves the sample from the first storing means. However, this feature is well known in the art as disclosed by Byrne et al., wherein it teach a analog to digital converter coupled to a buffer (a memory storage device) and the buffer coupled to a detector (Pat. No. 6, 487, 672; See Fig. 1, Elements 6, 20, 22). Shimada et al. and Byrne fail to teach wherein the second clock signal is faster than the first clock signal. However, this feature is well known in the art as disclosed by Sprague, wherein it teaches a recording device that has a FIFO memory wherein the information is clocked out at a rate higher than real time, but is clocked in at real time (Pat. No. 6, 072, 645; Col. 5, Lines 13-17). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the device to record in real time.

4. Claim 2, 6, 7, 8, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. Pat. No. 5, 056, 116), Byrne et al. (U. S. Pat. No. 6, 487, 672) and Sprague (US Patent No. 6, 072, 645) as applied to claim 1 above, and further in view of Leung et al. (U.S. Pat. No. 6, 546, 518).

Regarding Claim 2, Shimada et al., Byrne and Sprague disclose all the limitations of Claim 1. Shimada et al. fail to disclose that the apparatus data detecting part comprises a recursive process conducting part conducting a recursive process for the sample data retrieved from the first storing part in accordance with the predetermined algorithm so that maximum likelihood data is detected. However, this feature is known in the art as disclosed by Leung et al., wherein it teach a Viterbi detector that uses maximum likelihood data detection (Col. 1, Lines 35-44). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify

Shimada et al.'s invention in order for the detector to perform maximum likelihood detection of the data in order to improve the efficiency when performing data detection.

Regarding Claim 6, Shimada et al., Byrne Sprague and Leung et al. disclose all the limitations of Claim 2. Shimada et al. further teach wherein said recursive process conduction part conducts said recursive process based on an iterative number, which number is defined so that a required time required for completing said recursive process does not exceed a storing time required for storing the sample value by said first storing part (Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.).

Regarding Claim 7, Shimada et al., Byrne, Sprague and Leung et al. disclose all the limitations of Claim 2. Shimada et al. Byrne and Sprague fail to disclose recursive part conducts said recursive process based o the iterative number, which number in a case in which the recorded data is the data recorded in the data part. However, this feature is well known in the art as disclosed by Leung et al., wherein it teaches a recursive part conducts said recursive process based on the iterative number, which number in a case in which the recorded data is the data recorded in the data part (Pat. No. 6, 546, 518; Col. 2; Lines 19-42). It is obvious to a person of ordinary skill in the art to know that the process takes a certain amount of time and also that a detector is able to perform recursive processes (in other words, performs detections over and over again) when processing a signal.

Regarding Claim 8, Shimada et al., Byrne, Sprague Byrne and Sprague disclose all the limitations of Claim 2. Shimada et al. Byrne and Sprague fail to disclose recursive process conduction part conducts said recursive process based on an iterative number which number is defined so that a required time required completing said recursive process conducted does not exceed a scanning time required scanning a gap provided between an address part recording an address of data and a data part recording the data. However, this feature is well known in the art as disclosed by Leung et al., wherein it teaches a recursive process conduction part conducts said recursive process based on an iterative number which number is defined so that a required time required completing said recursive process conducted does not exceed a scanning time required scanning a gap provided between an address part recording an address of data and a data part recording the data (Pat. No. 6, 546, 518; Col. 2; Lines 19-42). It is obvious to a person of ordinary skill in the art to know that the process takes a certain amount of time and also that a detector is able to perform recursive processes (in other words, performs detections over and over again) when processing a signal.

Regarding Claim 12, Shimada et al. disclose an apparatus for reading recorded data, said apparatus comprising:

A first clock generating part generating a first clock signal and a second clock signal generating part generating a second clock signal different from the first clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.);

A sampling part sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal (Pat. No. 5, 056, 116; Col. 4, Lines 52-57);

A first storing part consecutively storing a sample value obtained by said sampling part (Pat. No. 5, 056, 116; See Fig. 22. Shimada et al. disclose that the analog to digital converter (Element 1) supplies the sampled signal to a buffer (Element 15), which is a storing part);

A data detecting part retrieving the sample value from said first storing part by synchronizing the second clock signal detecting data by processing the sample value in accordance with a predetermined algorithm, so that the recorded data is read based on the data detected by said data detecting part (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.).

Shimada et al. also disclose that the data detecting part is synchronized with a second clock signal synchronizing with a timing of storing the sample values to either said first storing part or said second storing part, whichever one has been switched by said first switching part (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector holds the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.). Shimada et al. also teach that the recorded data is data that is found in the data signal (See Abstract). Shimada et al. fail to disclose

that the detector retrieves the sample from the first storing means. However, this feature is well known in the art as disclosed by Byrne et al., wherein it teach a analog to digital converter coupled to a buffer (a memory storage device) and the buffer coupled to a detector (See Fig. 1, Elements 6, 20, 22). Shimada et al. and Byrne fail to teach wherein the second clock signal is faster than the first clock signal. However, this feature is well known in the art as disclosed by Sprague, wherein it teaches a recording device that has a FIFO memory wherein the information is clocked out at a rate higher than real time, but is clocked in at real time (Pat. No. 6, 072, 645; Col. 5, Lines 13-17). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the device to record in real time.

Regarding Claim 13, Shimada et al. disclose an apparatus for reading recorded data, said apparatus comprising:

A first clock generating part generating a first clock signal and a second clock signal generating part generating a second clock signal different from the first clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.);

A sampling part sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal (Pat. No. 5, 056, 116; Col. 4, Lines 52-57);

A first storing part consecutively storing a sample value obtained by said sampling part (Pat. No. 5, 056, 116; See Fig. 22. Shimada et al. disclose that the

analog to digital converter (Element 1) supplies the sampled signal to a buffer (Element 15), which is a storing part);

A data detecting part retrieving the sample value from said first storing part by synchronizing the second clock signal and detecting data by processing the sample value in accordance with a predetermined algorithm, so that the recorded data is read based on the data detected by said data detecting part (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.).

Shimada et al. also disclose that the data detecting part is synchronized with a second clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector holds the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.). Shimada et al. also teach that the recorded data is data that is found in the data signal (See Abstract). Shimada et al. further teach wherein said recursive process conduction part conducts said recursive process based on an iterative number, which number is defined so that a required time required for completing said recursive process does not exceed a storing time required for storing the sample value by said first storing part (Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.). Shimada et al. fail to disclose that the

detector retrieves the sample from the first storing means. However, this feature is well known in the art as disclosed by Byrne et al., wherein it teach a analog to digital converter coupled to a buffer (a memory storage device) and the buffer coupled to a detector (See Fig. 1, Elements 6, 20, 22). Shimada et al. and Byrne fail to teach wherein the second clock signal is faster than the first clock signal. However, this feature is well known in the art as disclosed by Sprague, wherein it teaches a recording device that has a FIFO memory wherein the information is clocked out at a rate higher than real time, but is clocked in at real time (Pat. No. 6, 072, 645; Col. 5, Lines 13-17). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the device to record in real time.

5. Claim 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al., Byrne et al. and Sprague as applied to claim 1 above, and further in view of Bushy, Jr. (U.S. Pat. No. 4, 896, 337) and Scheffler (US Pat. No. 5, 041, 921).

Regarding Claim 9, Shimada et al. and Byrne et al. disclose all the limitations of Claim 1. Shimada et al. and Byrne et al. fail to teach an apparatus comprising:

A first switching part switching to one of said first storing part and said second storing part; a second switching part switching to another one of said first storing part and said second storing part, which is not switched to by said first switching part;

Whereby one of said first storing part and said second storing part, which is switched to by said first switching part, stores the sample value, while said data detecting part retrieves the sample value from another one of said first storing part and said second storing part, which is switched to by said second switching part.

However, this feature is well known in the art as disclosed by Bushy, Jr., wherein it teaches an apparatus that has two different memory devices that receive the data and a switch between both memory devices (Pat. No. 4, 896, 337; See Fig. 3, Elements 30, 33, 41 and 42). Shimada et al. and Bushy et al. fail to teach a second storing part consecutively storing a sample value obtained by said sampling part. However, this feature is well known in the art as disclosed by Scheffler, wherein it teaches a output buffer receiving data from a first buffer (Pat. No. 5, 041, 921; Fig. 9, Elements 146 and 144, respectively. It is well known in the art that buffers store temporarily data.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the medium to have more than one memory device in order to control more efficiently the manipulation of data.

Regarding Claims 10 and 11, Shimada et al., Byrne et al. and Bushy, Jr. disclose all the limitations of Claim 9. Shimada et al., Byrne et al. and Bushy, Jr. fail to disclose data detecting part comprises a recursive process conducting part conducting a recursive process for the sample value, which is retrieved from one of said first storing part and said second storing part, which is switched by said second switching part, in accordance with the predetermined algorithm, and detecting the maximum likelihood data, by synchronizing with said second clock signal. It would have been obvious to a person of ordinary skill in the art, to combine two memory devices connected by a switch (Pat. No. 4, 896, 337; See Fig. 3, Elements 30, 33, 41 and 42) to be detected and processed by a detector (it is known that a detector performs recursive processes (in other words, performs detections over and over again) when processing a signal).

6. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. Pat. No. 5, 056, 116), Byrne et al. (U. S. Pat. No. 6, 487, 672), Sprague (US Pat. No.), Bushy, Jr. (U.S. Pat. No. 4, 896, 337) Scheffler (US Pat. No. 5, 041, 921) and Leung et al. (U.S. Pat. No. 6, 546, 518).

Regarding Claims 14 and 16, Shimada et al. disclose an apparatus for reading recorded data, said apparatus comprising:

A first clock generating part generating a first clock signal and a second clock signal generating part generating a second clock signal different from the first clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.);

A sampling part sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal (Pat. No. 5, 056, 116; Col. 4, Lines 52-57);

A first storing part consecutively storing a sample value obtained by said sampling part (Pat. No. 5, 056, 116; See Fig. 22. Shimada et al. disclose that the analog to digital converter (Element 1) supplies the sampled signal to a buffer (Element 15), which is a storing part);

A data detecting part retrieving the sample value from said first storing part by synchronizing the second clock signal and detecting data by processing the sample value in accordance with a predetermined algorithm, so that the recorded data is read based on the data detected by said data detecting part (Pat. No. 5, 056,

116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.).

Shimada et al. also disclose that the data detecting part is synchronized with a second clock signal (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.). Shimada et al. fail to disclose that the detector retrieves the sample from the first storing means. However, this feature is well known in the art as disclosed by Byrne et al., wherein it teach a analog to digital converter coupled to a buffer (a memory storage device) and the buffer coupled to a detector (Pat. No. 6, 487, 672; See Fig. 1, Elements 6, 20, 22). Shimada et al. and Byrne fail to teach wherein the second clock signal is faster than the first clock signal. However, this feature is well known in the art as disclosed by Sprague, wherein it teaches a recording device that has a FIFO memory wherein the information is clocked out at a rate higher than real time, but is clocked in at real time (Pat. No. 6, 072, 645; Col. 5, Lines 13-17). Shimada et al. Byrne and Sprague fail to disclose recursive process conduction part conducts said recursive process based on an iterative number which number is defined so that a required time required completing said recursive process conducted does not exceed a scanning time required scanning a gap provided between an address part recording an address of data and a data part recording the data. However, this feature is well known in the art as disclosed by Leung et al., wherein it teaches a

recursive process conduction part conducts said recursive process based on an iterative number which number is defined so that a required time required completing said recursive process conducted does not exceed a scanning time required scanning a gap provided between an address part recording an address of data and a data part recording the data (Pat. No. 6, 546, 518; Col. 2; Lines 19-42). However, this feature is well known in the art as disclosed by Bushy, Jr., wherein it teaches an apparatus that has two different memory devices that receive the data and a switch between both memory devices (Pat. No. 4, 896, 337; See Fig. 3, Elements 30, 33, 41 and 42). Shimada et al. and Bushy et al. fail to teach a second storing part consecutively storing a sample value obtained by said sampling part. Shimada et al., Byrne, Sprague and Leung et al. fail to teach of a first storing pat and a second storing part with a switch. However, this feature is well known in the art as disclosed by Scheffler, wherein it teaches a output buffer receiving data from a first buffer (Pat. No. 5, 041, 921; Fig. 9, Elements 146 and 144, respectively. It is well known in the art that buffers store temporarily data.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the medium to have more than one memory device in order to control more efficiently the manipulation of data.

Regarding Claims 15 and 17, Shimada et al., Byrne et al., Sprague, Bushy, Jr., Scheffler, Leung et al. teach all the limitations of Claim 14 and 16, respectively. Scheffler further teach wherein said iterative number is set when one of said first storing part and said second storing part, which one switched by said first switching part, stores the sample value of the address part (Pat. No. 5, 041, 921; Fig. 9, Elements 146 and 144, respectively. It is well known in the art that buffers store temporarily data.). It would

have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the medium to have more than one memory device in order to control more efficiently the manipulation of data.

Response to Arguments

Applicant's arguments filed 3/5/2004 have been fully considered but they are not persuasive. In Paper #6, filed 3/5/2004, Applicant added the feature of "A first clock generating part generating a first clock signal and a second clock signal generating part generating a second clock signal different from the first clock signal". However, Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller (Pat. No. 5, 056, 116; Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26.). Therefore, the Viterbi detector functioning as a first clock generating part and a second clock generating part because it samples and holds the first clock signal in order to generate a new clock signal, which is the second clock signal.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703)305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703)308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
May 6, 2004.

DAVID HUDSPETH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600